12. PET 4

1. Explanation of the sockets.

INT
VCC
Is the power supply from the machine to be used for the panel (normal operation), then the short circuiting bridge which is delivered with the machine, should be plugged between "INT" and "VCC".

Is an external voltage regulator to be used, then the short circuiting bridge should be plugged between "EXT" and "VCC".

VCC-EXT The voltage regulator should also be connected with the + (positive clamp) to the "VCC-EXT" and with the - (negative clamp) connected to "GND". The supply voltage should be + 5 volts + 5%. The "GND" socket is the Earth terminal with respect to the signal sockets.

CP1-T delivers a positive trigger impulse of ca. 8 us pulse width, when the machine programme, which is one the address switches of the Stop 1-addresses, is fed in. Which means, that the Stop 1 switch must be in the basic position, furthermore the selected address must be within the M1 cycle. For CP2-T, the same applies with reference to the Stop 2 addresses.

STP-EXT Zero potential on this signal input, brings the system into a Wait-State. The micro-programme is interrupted.

2. Explanation of the switches and keys.

Remarks: All switches (red) and all keys (black) have a preference (basic) position, into which they especially lightly switch.

Is the panel connected to the machine and are all the keys and switches in this (basic) position, then the free running of the machine through the panel should not be interrupted.

One can see, visually by means of the flickering indicator lamps, that the machine is running.

RESET By means of the "RESET" key, the system can be re-storted. The machine starts again with the programme step 0 (address 0).

CYCLE Is this switch activated, the system is interrupted. The programme remains in a Wait-State. This Wait-State can be in the 1st, 2nd or 3rd cycle of a command.

START

With the "START" key the programme can be followed, stepwise (cyclewise) as long as one has left the Wait-State (CYCLE-Switch activated). Furthermore one can, with this command, leave a started address which has been stopped or in the DMA-Fall, can switch the internal address counter further.

STOP1

These switches, when in the normal position, mean that the system does not follow an eventual STOP address (by means of the Address-Bit-Switch). On the sockets CP1-T and CP2-T a trigger pulse can be taken, as long as the programme of the set address travels and this lies in a M1 cycle. Is the STOP switch activated, then the system remains at the set address (in the Wait-State) as long as the programme has reached the STOP address.

Address switch AØ-A15 By means of these switches, the respective STOP and Trigger addresses between 0 and 64K can be selected, both at the same time (STOP1-TRIG1/STOP2-TRIG2).

With the switches in the normal position ADDRESSBIT "LOW" With the switches in the working position ADDRESSBIT "HIGH" With the address switch row 2 (STOP2), the addresses for "DMA" operation can be set.

DMA

With this switch one effects the so called "DMA" operation (DIRECT MEMORY ADDRESS). Is this switch activated, then the CPU carries out the current command and goes eventually into the so called TRI-STATE. This means, that the memory media which are contained in the machine are separated from the CPU and can be directly utilized from the panel. This allows the memory contents to be read directly from the panel and also allows the accessible contents to be changed without using the CPU. If one leaves the HOLD-STATE in that the "DMA" switch is brought again into the normal position, then the CPU continues the programme from the point where it was interrupted.

MEM-I/O

This switch controls the DMA-Fall, if the DMA is to be made from the memory or with the I/O-PORTS.

WRITE

Is this switch in the normal position, this means that in the DMA-Fall, from the memory or I/O PORT is being read. If one switches into the WRITE position, so is in the addressed byte every Data bit pattern written, which is selected by means of the Data bit switch DØ-D7, the precondition is however, that the address selected is in the accessible memory range (RAM) of the system or an OUTPUT-PORT with LATCH quality is addressed.



3. Explanation for the Indicator lamps (LED)

ADDRESS LAMPS AØ-A15	Indicate the immediate condition of the Addressingbus. Illuminated LED means Address Bit "HIGH". Non-illuminated Address Bit "LOW". A plottable value of the indication is only available, when the system is in the waiting condition (Wait or Halt-State, DMA).								
DATA- LAMPS DØ-D7	Show the condition of the DATABUS. Otherwise the conditions are the same as for the ADDRESS lamps.								
CPU-STA TUS LAMPS	Show the momentary condition of the CPU.								
WATT	The CDI is in the WHATT STATEM TO THE STATEM								

WAIT	The CPU is in	the "WAIT-STATE".	The system is	conditioned
	and waits.		,	

WR	The LED shows, that the CPU is in the transmit condit.	ion
	(e.g. writing into the memory)	

DPIN	The CPU is switched to receive. CPU, when the LED lights.	The Data	flows	into	the
	or of which the LED rights.				

DMA The illuminated LED shows that the CPU is in the TRI-STATE (HOLD-) condition.

INTE The INTE-LED shows when the CPU can accept an INTERRUPT signal.

SYSTEM- Show the momentary condition of the system. STATUS LAMPS

MEMW Is this lamp illuminated, then information is being written into the memory.

MEMR Is this lamp illuminated, then is the system in the Memory read cycle.

IOW Is this LED illuminated, then information is being written in an OUTPUT-PORT.

IOR The LED illuminates, when an INPUT-PORT is an Interrogate.

Is this LED illuminated, then is the system in the 1.byte command condition. This is always a Memory-Read M1

cycle.

This means that the LED's "MEMR" and "DBIN" will also

be illuminated.

The STACK-LED shows that the system is in a STACK-CYCLE. **STACK** Normally in the STACK, return addresses are stored.

This LED shows, when after an INTERRUPT, this is **INTA**

recognized and accepted by the CPU.

MAGNETIC TAPE COMMANDS

Mnemo Code	OP Code	I	Į II	III	IV	٧	Number of Groups
OPI	48	g	ia	vr			3
OPO	49	g	ia	٧r			3
GET	50	g	ia	ср			
-	_	ia	r	b			6
PUT	51	g	ia	ср			
-	-	ia	r	b			6
SEK	52	g	ia	٧r			3
MRK	53	g	ia	٧r			3
SKP	54	g	ia	ср			3
CLS	56	g	ia	٧r			3
ERS	57	g	s				2
BCK	60	g	ia	vr			3
OBO	61	g	ia	vr			3
OBI	62	g	ia	vr			3
LEDGER	CARD C	OMMAN	DS				
OPN	48	g	ia	vr			3
GET	50	g	ia .	ср			6
-	_	ia	r	b			O
PUT	51	g	ia	ср			
-	_	ia	r	b			6
TLM	52	g	zp				2
TLN	53	g	zp				2
LFL	54	g	ia	fl			3
LLJ	55	g	ia	sp			3
REP-COM	IMAND FO	OR MA	GNETIC T	APE AND	LEDGER	CARDS	
Mnemo Code	OP Code	Ι	II	III	IV	V	Number of Groups
REP	59	g	ia	vr			3

BASIC MACHINE COMMANDS

Mnemo Code	OP Code	I	II	III	IV	٧	Number of Groups
TRV BRV ADD MUL NUR MVD MVR	00 01 02 03 04 05 06	- * - sr sr dc dc	ia ia vr vr vr vr	Vr Vr Vr			3 3 2 2 2 2 2
TST DIV SHL SHR CCN OPS JUN	08 09 10 11 12 13 16	sl sl sr - O ps	x vr vr vr ai n	co m	со		2 or 3 2 2 2 2 3 or 4 1,2 or 3
JM1 JM2 JM3 JM4 JM5 JM6 JMS RET	17 18 19 20 21 22 24 25	ps ps ps ps ps ps	<=>	m	f	lv	1 1 1 1 1 1 4 or 5
JME JML	26 27	ps ps		""		10	1 1
JMM SET RST WAK MAK MAT OUP OUT PRA ACP TAB LIN COL NOP MVA	23 29 30 32 33 34 40 41 42 43 45 46 47 63 07	ps m cp cp ac nu sy cp ia j1/j2 j1/j2 j1/j2 O	1 ai mia vu nk vr kl pc sp	ky ky vr vk cp cp	th	tl	1 2 2 3 3 5 3 2 3 2 3 2 3 1
_	_	ia ia	r	b b			8
CPA - -	35 - -	ia ia ia	cp r r	b b			8
PRL - PCK	36 - 38	ia ia ia	cp r cp	b			5
- UPK	- 39	ia sy	r nk	b cp b			5 6
ACS	- 44 -	ia ia ia	r np r	b cp b			6

	(COCL O) - to common ord - su	ı	r = Data progr.memory area	s = Clear 1m Tape on MBK	sl = Rounding off (max.15)	sp = Jump line	ı	ı	sy = symbol	th = Highest sengrator		tl = Lowest separator	u = And combination		<pre>vk = Fre-decimal points</pre>	vr = Data memory	VII Pro Dro III	Ī	x = Auxiliary cell 1 or 2	zp = Line position (0-2)
			,	(er)							7		_	•		_	,		×	N
	= 1st EF	= 2nd FF				= Start key (1 – 6)	: Lamp (1 - 4)	: Line feed		<pre>: Subroutine levels (max.4)</pre>			Standard print	Decimal points			Zero suppression / che		5	Position counter (max. 192)
		2 =			"		II				II		II	11			11	I		II
	ij		11/12	7, 7, 7	¥ .	K	-	lc	-	> T	Ε	1	_	감	2	<u>-</u>	n	С		ဝ
Explanation of the Abbreviations	a	= Negative	= Total	= (For marker) <>			= Accu (data memory 0)	= Alpha input	= Byte address (0 = 3071)		= Constant	= Capacity (may 255)		= Decade	= Error routine		= rorm lenght (max 112)	= Device number $(0 - 3)$	Indirect address:	
EXP		T	*	٨			o O	 	 P		00	CD		u op	" +	£1	- -	g	ia	
														-	350			٠,		1.5